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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,130	03/23/2004	Carrell W. Ewing	40026XY	2108

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EXAMINER	
PATEL, ASHOKKUMAR B	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,130	EWING ET AL.	
	Examiner	Art Unit	
	Ashok B. Patel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *1-5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/16/05,2/16/05,7/13/2004*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Application Number 10/806, 130 was filed on 03/23/2004. Claims 6-38 are subject to examination. Claims 1-5 are canceled.

Priority

2. An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence(s) of the specification or in an application data sheet by identifying the prior application by application number (37 CFR 1.78(a)(2) and (a)(5)). If the prior application is a non-provisional application, the specific reference must also include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

3. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120 as follows:

The later-filed application must be an application for a patent for an invention which is also disclosed in the prior application (the parent or original nonprovisional application or provisional application); the disclosure of the invention in the parent application and in the later-filed application must be sufficient to comply with the requirements of the first paragraph of 35 U.S.C. 112. See *Transco Products, Inc. v. Performance Contracting, Inc.*, 38 F.3d 551; 32 USPQ2d 1077 (Fed. Cir. 1994).

Referring to claims 6, 21 and 36,

The instant application's incorporation of "a power supply housing " and "a plurality of power outlets mounted in the power supply housing" and "a plurality of power outlets"

which Examiner was unable to locate in the applications 10/758, 117, 09/375, 471 and 08/685, 436. And as such, the priority date for claims 6, 21 and 36 was considered as being 03/23/2004.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6, 7, 9-14, 21, 22, 24-29 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reynolds et al. (hereinafter Reynolds) (US 2004/0047095 A1) and in view of "Official Notice"

Referring to claim 6,

The reference teaches a network power manager apparatus of the type useable in a computer network having a host system with a network power manager application (Fig. 29) adapted to issue network commands and communicate network commands (Figs 1-21) over a network communications connection supporting IP communications (page 3, para. [0049]), the network power manager apparatus comprising in combination:

a power supply housing (Fig.22B);

a power manager agent application mounted in association with the housing and being connectable to the network communications connection (Fig.24, page 7, para. [0131]);

a plurality of power outlets mounted in the power supply housing (Fig. 22B);

The reference Reynolds teaches in Fig. 24, logic modules (page 7, para. [0131]) including microprocessor that is being adapted to provide power from a power source to a corresponding power outlet among the plurality of power outlets and being in communication with said power manager agent application to provide power cycling on-off of said corresponding power outlet and at least one of power state sensing and load-sensing with respect to said corresponding power outlet in response to one or more commands. (Page 3, Table 1, please refer to column "TCP/IP-SNMP"). The reference further teaches on page 7, para. [0129], "As a further example, one or more of the controlled power outlets can be controlled together, such as a system providing four pairs of power outlets.".

The reference fails to explicitly teach a plurality of intelligent power modules mounted in the power supply housing. However 'Official Notice' is taken by the Examiner that a plurality of Fig. 24, logic modules (page 7, para. [0131]) can be provided as each Fig. 24, logic modules (page 7, para. [0131]) is dedicated to control the corresponding outlet individually. It would have been obvious to one having ordinary skill in art at the time of invention was made to provide a dedicated Fig. 24, logic modules (page 7, para. [0131]) (intelligent power module) for each outlet, rather than just one "intelligent power module" controlling all the outlets because a theory of distributed processing allows division of calculations amongst a multiplicity of slower computers and the results of the separate computations are combined into one, thereby achieving the result in the same time as the faster computer, but with slower speed lower cost processors than a more expensive one. It also allows the elimination of data

multiplexing and minimizing the presence of signals on the electrical interconnection. (**Note:** Also It has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. Nerwin v. Erlichman, 168 USPQ 177, 179.)

Referring to claims 7 and 22,

The reference teaches the network power manager apparatus further comprising a serial communications connection supported by a microprocessor, said serial communications connection connecting each of the intelligent power modules to the power manager agent application. (page 3, para. [0045] and [0046])

Referring to claims 9 and 24,

The reference Reynolds teaches the network power manager apparatus wherein said microprocessor communicates the power-on status of the IPM-corresponding outlet to the network power manager application through said power manager agent application as a variable in a managed information base data construct communicated over the network communications connection in accordance with a predefined simple network management protocol. (Page 3, Table 1, please refer to column "TCP/IP-SNMP").

Referring to claims 10 and 25,

The reference Reynolds teaches a microprocessor connected by a load sensor that independently senses the load status of the corresponding outlet. (Fig. 24, element "Current sensors", Page 3, Table 1, please refer to column "TCP/IP-SNMP").

The reference fails to explicitly teach a plurality of intelligent power modules mounted in the power supply housing. However 'Official Notice' is taken by the

Examiner that a plurality of Fig. 24, logic modules (page 7, para. [0131]) can be provided as each Fig. 24, logic modules (page 7, para. [0131]) is dedicated to control the corresponding outlet individually. It would have been obvious to one having ordinary skill in art at the time of invention was made to provide a dedicated Fig. 24, logic modules (page 7, para. [0131]) (intelligent power module) for each outlet, rather than just one "intelligent power module" controlling all the outlets because a theory of distributed processing allows division of calculations amongst a multiplicity of slower computers and the results of the separate computations are combined into one, thereby achieving the result in the same time as the faster computer, but with slower speed lower cost processors than a more expensive one. It also allows the elimination of data multiplexing and minimizing the presence of signals on the electrical interconnection. (**Note:** Also It has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. Nerwin v. Erlichman, 168 USPQ 177, 179.)

Referring to claims 11 and 26,

The reference Reynolds teaches the network power manager apparatus wherein said microprocessor is adapted to communicate the load status to the network power manager application through the power manager agent application as a variable in a managed information base (MIB) data construct communicated over the network communications connection in accordance with a predefined simple network management protocol (SNMP). (Page 3, Table 1, please refer to column "TCP/IP-SNMP", page 4, para.[0064]-[0066]).

Referring to claims 12 and 27,

The reference Reynolds teaches a microprocessor in communication with a relay that independently controls the power applied to the corresponding outlet. (Fig. 24, element "Relays", Fig. 27, elements KO, K1, K2)

The reference fails to explicitly teach a plurality of intelligent power modules mounted in the power supply housing. However 'Official Notice' is taken by the Examiner that a plurality of Fig. 24, logic modules (page 7, para. [0131]) can be provided as each Fig. 24, logic modules (page 7, para. [0131]) is dedicated to control the corresponding outlet individually. It would have been obvious to one having ordinary skill in art at the time of invention was made to provide a dedicated Fig. 24, logic modules (page 7, para. [0131]) (intelligent power module) for each outlet, rather than just one "intelligent power module" controlling all the outlets because a theory of distributed processing allows division of calculations amongst a multiplicity of slower computers and the results of the separate computations are combined into one, thereby achieving the result in the same time as the faster computer, but with slower speed lower cost processors than a more expensive one. It also allows the elimination of data multiplexing and minimizing the presence of signals on the electrical interconnection. (**Note:** Also It has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. Nerwin v. Erlichman, 168 USPQ 177, 179.)

Referring to claims 13 and 28,

The reference Reynolds teaches the network power manager apparatus wherein said microprocessor controls the power applied to the corresponding outlet (page 4, para.[0066], "Per-outlet current monitoring according to specific embodiments of the invention provides a mechanism of remotely managing current load on a individual device basis.") in response to a variable in a managed information base (MIB) data construct communicated from the network power manager application to the power manager agent application over the network communications connection in accordance with a predefined simple network management protocol (SNMP). (Page 3, Table 1, please refer to column "TCP/IP-SNMP").

Referring to claims 14 and 29,

The reference Reynolds teaches the network power manager apparatus with a microprocessor in communication with: a power state sensor that independently senses the power-on status of the corresponding outlet; a load sensor that independently senses the load status of the corresponding outlet; (Fig. 24, element "Sensors", Page 3, Table 1, please refer to column "TCP/IP-SNMP") and a relay that independently controls the power applied to the corresponding outlet. (Fig. 24, element "Relays", Fig. 27, Fig. 27, elements KO, K1, K2)

Referring to claim 21,

The reference Reynolds teaches a network power manager apparatus of the type useable in a computer network having a host system with a network power manager application (Fig. 29) adapted to issue network commands and communicate network

commands (Figs. 1-21) over a network communications connection (page 3, para.[0049]), the network power manager apparatus comprising in combination:

a power manager agent application connectable to the network communications connection(Fig. 24, page 7, para.[0131]);

a plurality of power outlets (Fig. 22B)

The reference Reynolds teaches in Fig. 24, logic modules (page 7, para. [0131]) including microprocessor that is being adapted to provide power from a power source to a corresponding power outlet among the plurality of power outlets and being in communication with said power manager agent application to provide power cycling on-off of said corresponding power outlet and at least one of power state sensing and load-sensing with respect to said corresponding power outlet in response to one or more commands. (Page 3, Table 1, please refer to column "TCP/IP-SNMP"). The reference further teaches on page 7, para.[0129], "As a further example, one or more of the controlled power outlets can be controlled together, such as a system providing four pairs of power outlets.".

The reference fails to explicitly teach a plurality of intelligent power modules mounted in the power supply housing. However 'Official Notice' is taken by the Examiner that a plurality of Fig. 24, logic modules (page 7, para. [0131]) can be provided as each Fig. 24, logic modules (page 7, para. [0131]) is dedicated to control the corresponding outlet individually. It would have been obvious to one having ordinary skill in art at the time of invention was made to provide a dedicated Fig. 24, logic modules (page 7, para. [0131]) (intelligent power module) for each outlet, rather

than just one "intelligent power module" controlling all the outlets because a theory of distributed processing allows division of calculations amongst a multiplicity of slower computers and the results of the separate computations are combined into one, thereby achieving the result in the same time as the faster computer, but with slower speed lower cost processors than a more expensive one. It also allows the elimination of data multiplexing and minimizing the presence of signals on the electrical interconnection. (**Note:** Also It has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. Nerwin v. Erlichman, 168 USPQ 177, 179.)

Referring to claim 36,

The reference Reynolds teaches a network power manager apparatus of the type useable in a computer network having a host system with a network power manager application (Fig. 29) adapted to issue network commands and communicate network commands (Figs. 1-21) over a network communications connection supporting IP communications (page 3, para.[0049]), the network power manager apparatus comprising in combination:

a power supply housing (Fig. 22B);

a power manager agent application mounted in the housing and being connectable to the network communications connection(Fig. 24, page 7, para.[0131]);

a plurality of power outlets mounted in the power supply housing (Fig. 22B);

The reference Reynolds teaches in Fig. 24, logic modules (page 7, para. [0131]) including microprocessor that is being adapted to provide power from a power source to

a corresponding power outlet among the plurality of power outlets and being in communication with said power manager agent application to provide power cycling on-off of said corresponding power outlet and at least one of power state sensing and load-sensing with respect to said corresponding power outlet in response to one or more commands. (Page 3, Table 1, please refer to column "TCP/IP-SNMP"). The reference further teaches on page 7, para.[0129], "As a further example, one or more of the controlled power outlets can be controlled together, such as a system providing four pairs of power outlets.". The reference Reynolds teaches sensors in Fig. 24, element "Sensors" and Page 3, Table 1, please refer to column "TCP/IP-SNMP", Fig. 28A) (thereby the reference teaches said power state sensor having a voltage state determination processor in voltage determination communication with a power relay in power controlling communication with said corresponding power outlet. said intelligent power module being in power state reporting communication with the network power manager application through said power manager agent application through one or more variables in a managed information base data construct communicated over the network communications connection in accordance with a predefined simple network management protocol.

The reference fails to explicitly teach a plurality of intelligent power modules mounted in the power supply housing. However 'Official Notice' is taken by the Examiner that a plurality of Fig. 24, logic modules (page 7, para. [0131]) can be provided as each Fig. 24, logic modules (page 7, para. [0131]) is dedicated to control the corresponding outlet individually. It would have been obvious to one having

ordinary skill in art at the time of invention was made to provide a dedicated Fig. 24, logic modules (page 7, para. [0131]) (intelligent power module) for each outlet, rather than just one "intelligent power module" controlling all the outlets because a theory of distributed processing allows division of calculations amongst a multiplicity of slower computers and the results of the separate computations are combined into one, thereby achieving the result in the same time as the faster computer, but with slower speed lower cost processors than a more expensive one. It also allows the elimination of data multiplexing and minimizing the presence of signals on the electrical interconnection. (**Note:** Also It has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. Nerwin v. Erlichman, 168 USPQ 177, 179.)

Referring to claim 37,

The reference Reynolds teaches the network power manager apparatus of claim 36 in which the voltage state determination processor (Page 3, Table 1, please refer to column "TCP/IP-SNMP", Fig. 24, element "sensors"). comprises a microprocessor portion controllably communicating with said power relay (Fig. 24, elements "Rabbit 2000 Microprocessor & Memory" and "Relay").

Referring to claim 38,

The reference Reynolds teaches the network power manager apparatus of claim 37 in which the network communications connection is a serial connection providing serial communication between the network power manager application and the power manager agent application. (page 4, para.[0071],[0072])

6. Claims 8, 23, 15-20, and 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reynolds et al. (hereinafter Reynolds) (US 2004/0047095 A1) and in view of "Official Notice" as applied to claim 6 above, and further in view of Ewing et al. (hereinafter Ewing)(US 5, 506, 573)

Referring to claims 8 and 23,

Keeping in mind the teachings of the reference Reynolds as stated above, the reference fails to explicitly teach a plurality of intelligent power modules mounted in the power supply housing. However 'Official Notice' is taken by the Examiner that a plurality of Fig. 24, logic modules (page 7, para. [0131]) can be provided as each Fig. 24, logic modules (page 7, para. [0131]) is dedicated to control the corresponding outlet individually. It would have been obvious to one having ordinary skill in art at the time of invention was made to provide a dedicated Fig. 24, logic modules (page 7, para. [0131]) (intelligent power module) for each outlet, rather than just one "intelligent power module" controlling all the outlets because a theory of distributed processing allows division of calculations amongst a multiplicity of slower computers and the results of the separate computations are combined into one, thereby achieving the result in the same time as the faster computer, but with slower speed lower cost processors than a more expensive one. It also allows the elimination of data multiplexing and minimizing the presence of signals on the electrical interconnection. (**Note:** Also It has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. Nerwin v. Erlichman, 168 USPQ 177, 179.)

However, both of these references fails to teach wherein each intelligent power module further comprises a microprocessor connected by an opto-isolator whereby the intelligent power module may independently sense the power state of said corresponding outlet. The reference Ewing teaches a microprocessor connected by an opto-isolator whereby the intelligent power module may independently sense the power state of said corresponding outlet (Fig. 1, element 48). Therefore it would have been obvious to one having ordinary skill in art at the time of invention was made to provide an opto-isolator between the intelligent power module whereby the intelligent power module may independently sense the power state of said corresponding outlet since input to output circuit isolation has been widely achieved through the use of opto-isolators. It is necessary such that the outlet voltages (120 V) needs to be isolated from the intelligent power module which is operating at 5 V power supply, as taught by Reynolds in Fig. 24, to avoid the damage caused by higher voltages to the intelligent power module.

Referring to claims 15-20 and 30-35,

Keeping in mind the teachings of the reference Reynolds, the reference Reynolds teaches sensors in Fig. 24, element "Sensors" and Page 3, Table 1, please refer to column "TCP/IP-SNMP", Fig. 28A) (thereby the reference teaches wherein said power state sensor comprises a voltage state determination processor in voltage determination communication with a power relay in power controlling communication with said corresponding power outlet.)

The reference fails to explicitly teach a plurality of intelligent power modules mounted in the power supply housing. However 'Official Notice' is taken by the Examiner that a plurality of Fig. 24, logic modules (page 7, para. [0131]) can be provided as each Fig. 24, logic modules (page 7, para. [0131]) is dedicated to control the corresponding outlet individually. It would have been obvious to one having ordinary skill in art at the time of invention was made to provide a dedicated Fig. 24, logic modules (page 7, para. [0131]) (intelligent power module) for each outlet, rather than just one "intelligent power module" controlling all the outlets because a theory of distributed processing allows division of calculations amongst a multiplicity of slower computers and the results of the separate computations are combined into one, thereby achieving the result in the same time as the faster computer, but with slower speed lower cost processors than a more expensive one. It also allows the elimination of data multiplexing and minimizing the presence of signals on the electrical interconnection. (**Note:** Also It has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. Nerwin v. Erlichman, 168 USPQ 177, 179.)

However, both of these references fails to teach a power supply and clock generator, connected to a load-sensor, a power state sensor, and a relay and that applies a series of alternating current (AC) voltage pulses synchronized to a source of AC power to the corresponding outlet with an on/off switch, said load sensor being adapted to sense the presence of a series of AC current pulses that result if said on/off switch is closed; a microprocessor that analyzes any AC current pulses detected by said load sensor to determine if they resulted from application of the AC voltage pulses;

and an input/output connection connected to said microprocessor that outputs an on/off status indication for said switch, and wherein each intelligent power module further comprises: power output terminals with a power switch; a synchronized pulse generator connected to said terminals that applies an alternating pulsed voltage synchronized to an incoming alternating current power source to the corresponding outlet; a load sensor connected in series with said terminals and said power supply/clock generator; and a microprocessor connected to both said synchronized pulse generator and the load sensor, said microprocessor being adapted to determine if a current sensed by said load sensor resulted from both said switch being closed and application of the alternating pulsed voltage from said synchronized pulse generator, and wherein said synchronized pulse generator further comprises a clock generator with an output that coincides with each zero-crossing of the incoming alternating current power, and wherein said load sensor further comprises an opto-isolator and a sense resistor, and wherein said microprocessor further comprises a data input connected to said opto-isolator and a data output connected to control the synchronized pulse generator.

The reference Ewing teaches these elements in Fig.1, Fig. 2 and col.3, line 11through col. 4, line 26) . Therefore it would have been obvious to one having ordinary skill in art at the time of invention was made to provide a dedicated Fig. 24, logic modules (page 7, para. [0131]) (intelligent power module) for each outlet, rather than just one "intelligent power module" controlling all the outlets because a theory of distributed processing allows division of calculations amongst a multiplicity of slower computers and the results of the separate computations are combined into one, thereby

achieving the result in the same time as the faster computer, but with slower speed lower cost processors than a more expensive one. It also allows the elimination of data multiplexing and minimizing the presence of signals on the electrical interconnection and sensing of whether an appliance on the network is off can be automatically turned on as taught by Ewing.

Conclusion

Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (571) 272-3972. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abp
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